What is claimed:

1. A semiconductor device comprising:

a pad section over an interlayer dielectric layer,

wherein the interlayer dielectric layer includes a first silicon oxide layer that is formed by a polycondensation reaction of a silicon compound and hydrogen peroxide, and a second silicon oxide layer formed over the first silicon oxide layer and containing an impurity, and

the pad section includes a wetting layer and a metal wiring layer.

2. A semiconductor device according to claim 1, wherein the impurity contained in the second silicon oxide layer is phosphorous.

3. A semiconductor device according to claim 1, wherein the metal wiring layer is formed from aluminum or an aluminum alloy.

4. A semiconductor device according to claim 1, wherein the wetting layer is formed from a material that is selected from titanium, cobalt, zirconium, silicon and niobium.

5. A semiconductor device according to claim 1, wherein the metal wiring layer includes an alloy layer that contacts the wetting layer, the alloy layer including a material that forms the wetting layer and a material that forms the metal wiring layer.

6. A semiconductor device according to claim 5, wherein the alloy layer has a film thickness that is two to three times greater than a film thickness of the wetting layer.

7. A semiconductor device according to claim 1, wherein the pad section does not have a nitride layer.

8. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming a interlayer dielectric layer, the step including:

(a) (1) forming a first silicon oxide layer by reacting a silicon compound and hydrogen peroxide through a chemical vapor deposition method, and

(a) (2) forming a second porous silicon oxide layer by reacting a silicon compound, at least one of oxygen and a compound including oxygen, and a compound including an impurity through a chemical vapor deposition method;

(b) forming a wetting layer over the interlayer dielectric layer;

(c) forming a metal wiring layer over the wetting layer; and

(d) forming a pad section by patterning the wetting layer and the metal wiring layer.

9. A method for manufacturing a semiconductor device according to claim 8, further comprising, after the step (a), the step of conducting an anneal treatment at a temperature of 600 – 850°C.

10. A method for manufacturing a semiconductor device according to claim 8, wherein the silicon compound used in the step (a) (1) is at least one type selected from an inorganic silane compound including monosilane, disilane, SiH_2Cl_2 and SiF_4, or an organo silane compound including CH_3SiH_3, tripropyl-silane and tetraethylorthosilicate.

11. A method for manufacturing a semiconductor device according to claim 8, wherein the step (a) (1) is conducted with the silicon compound being an inorganic silane compound by a reduced pressure chemical vapor deposition method at a temperature of 0 – 20°C.

12. A method for manufacturing a semiconductor device according to claim 8, wherein the step (a) (1) is conducted with the silicon compound being an organo silane compound by a reduced pressure chemical vapor deposition method at a temperature of 100 – 150°C.

13. A method for manufacturing a semiconductor device according to claim 8, wherein the step (a) (2) is conducted by a plasma chemical vapor deposition method at a temperature of 300 – 450°C.

14. A method for manufacturing a semiconductor device according claim 13, wherein the compound including oxygen used in the step (a) (2) is dinitrogen monoxide.

15. A method for manufacturing a semiconductor device according to claim 8, wherein the step (a) (2) is conducted by a chemical vapor deposition method at a temperature of 300 – 550°C.

16. A method for manufacturing a semiconductor device according to claim 15, wherein the compound including oxygen used in the step (a) (2) is ozone.

17. A method for manufacturing a semiconductor device according to claim 8, wherein, before forming the second silicon oxide layer in the step (a) (2), the first silicon oxide layer is exposed to an ozone atmosphere.

18. A method for manufacturing a semiconductor device according to claim 8, wherein the impurity used in the step (a) (2) is phosphorous.

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19. A method for manufacturing a semiconductor device according to claim 8, wherein the metal wiring layer is provided by forming a first aluminum layer including aluminum or an alloy containing aluminum as a main component at a temperature of 200°C or lower, then forming a second aluminum layer including aluminum or an alloy containing aluminum as a main component at a temperature of 300°C or higher.

20. A method for manufacturing a semiconductor device, comprising:

forming a first silicon oxide layer using a polycondensation reaction of a silicon compound and hydrogen peroxide;

forming a second silicon oxide layer including an impurity therein; and

forming a pad section over the first silicon oxide layer and the second silicon oxide layer, the pad section including a wetting layer and a wiring layer.

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21. A method as in claim 20, comprising forming the second silicon oxide layer to be more porous than the first silicon oxide layer.